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**Department of Computer Science and Engineering**

**Topic: Basic and Universal Gates -iVerilog**

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**Sub Code:** 19CSE211 **Sub Title:** Computer Organization and Architecture

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**Activity No:1 Date:11-01-2021**

1. **OR GATE :**

module orgate (a,b,y);

input a,b;

output y;

assign y= a| b;

endmodule

**Test bench:**

module orgate\_tb;

wire t\_y;

reg t\_a, t\_b;

orgate my\_gate( .a(t\_a), .b(t\_b), .y(t\_y) );

initial

begin

$monitor(t\_a,t\_b,t\_y);

t\_a = 1'b0;

t\_b = 1'b0;

#5

t\_a = 1'b0;

t\_b = 1'b1;

#5

t\_a = 1'b1;

t\_b = 1'b0;

#5

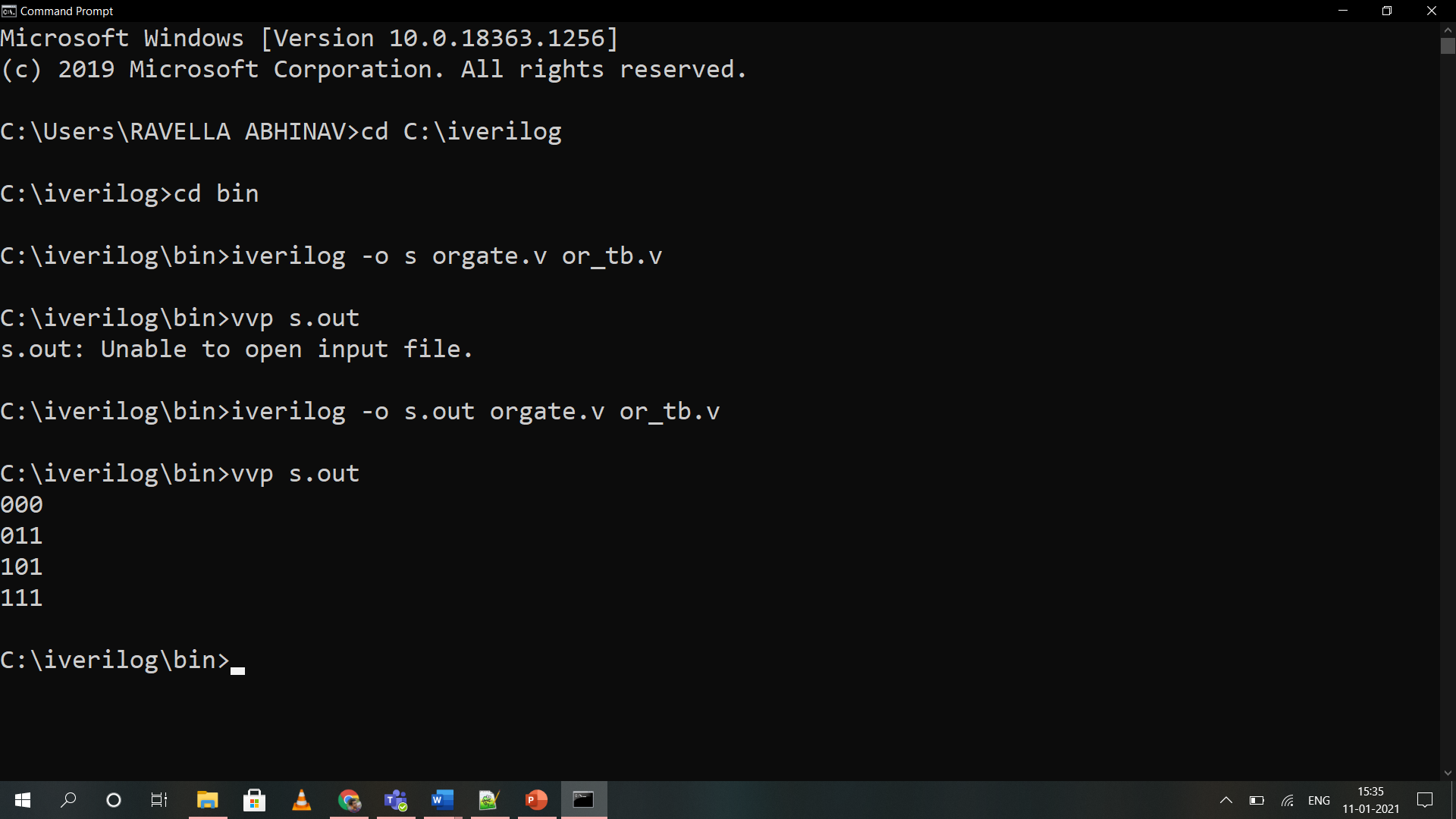
t\_a = 1'b1;

t\_b = 1'b1;

end

endmodule

**Output:**



**2.)AND GATE:**

module andgate (a, b, y);

input a, b;

output y;

assign y = a & b;

endmodule

**Test bench:**

module andgate\_tb;

wire t\_y;

reg t\_a, t\_b;

andgate my\_gate( .a(t\_a), .b(t\_b), .y(t\_y) );

initial

begin

$monitor(t\_a, t\_b, t\_y);

t\_a = 1'b0;

t\_b = 1'b0;

#5

t\_a = 1'b0;

t\_b = 1'b1;

#5

t\_a = 1'b1;

t\_b = 1'b0;

#5

t\_a = 1'b1;

t\_b = 1'b1;

end

endmodule

**Output:**



**3.)NOT GATE:**

module notgate (a,y);

input a;

output y;

assign y = !a;

endmodule

**Test bench:**

module notgate\_tb;

wire y;

reg a;

notgate my\_gate( .a(a),.y(y) );

initial

begin

$monitor(a,y);

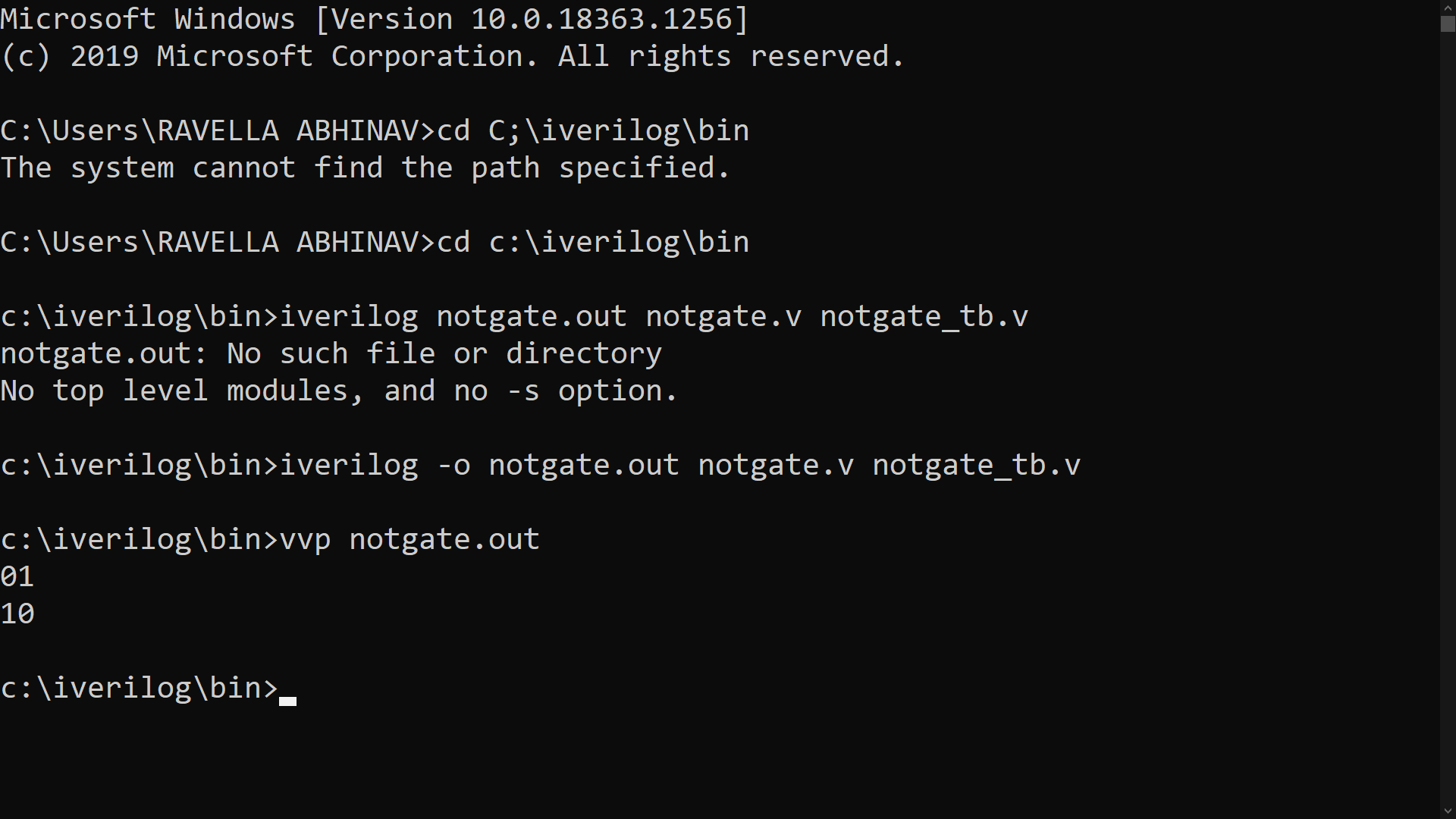
a=1'b0;

#10

a=1'b1;

end endmodule

**Output:**



**4.)NAND GATE:**

module nand\_gate(c,a,b);

input a,b;

output c;

nand (c,a,b);

endmodule

**Test Bench:**

module nand\_test;

reg a,b;

wire c;

nand\_gate nand\_test(c,a,b);

initial

begin

#000 a=0;b=0;

#100 a=0;b=1;

#100 a=1;b=0;

#100 a=1;b=1;

end

initial

begin

$monitor("a=%b,b=%b,c=%b",a,b,c);

end

endmodule

**Output:**

